RF NONLINEAR DEVICE CHARACTERIZATION YIELDS IMPROVED MODELING ACCURACY

Mark A. Smith, Thomas S. Howard

Kevin J. Anderson, and Anthony M. Pavio

Texas Instruments Incorporated

ABSTRACT

A new method for measuring the nonlinear characteristics of microwave GaAs field-effect transistors (FETs) has been developed and evaluated. The technique, which involves RF rather than DC FET measurement, has yielded significant improvement in circuit compression point and harmonic content modeling accuracy.

INTRODUCTION

The nonlinear circuit modeling method employed is the modified harmonic balance technique previously described by Peterson et. al. (1). Figure 1 is a schematic diagram of the amplifier circuit considered. The transistor itself is composed of the usual linear resistors, capacitors, and inductors, as well as the three nonlinear current sources I_D, I_G, and I_B. Of these current sources, I_D is the most significant, as it represents the familiar drain current vs. gate and drain voltage characteristics shown in Figure 2. I_G and I_D are highly nonlinear Schottky gate and reverse breakdown currents that flow only in extreme gate and drain voltage excursions. The matching networks present on the gate and drain have been reduced to equivalent linear impedances, and the feedback network, if any, has been represented by the two-port admittance matrix Y_F.

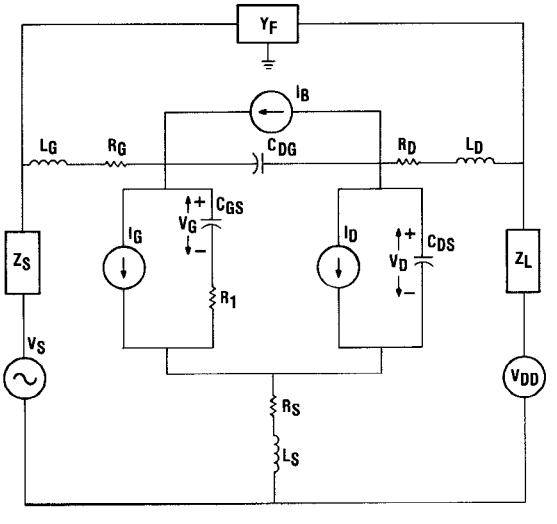

Figure 1. Circuit model for the large-signal FET analysis program.

The I_D current source, which is a function of both the gate and drain voltages, is represented in the nonlinear modeling programs as tabular data derived from actual FET measurements. These tabular data contain information about both the transconductance, G_M, and the equivalent output resistance R_{DS}, of the FET. G_M is defined as $\delta I_D/\delta V_G$ with constant V_D (assuming that the parasitic resistances R_G, R_S and R_D are zero) and the output conductance of the device, G_{DS}, is $\delta I_D/\delta V_D$ with constant V_G. The slope of the curves shown in Figure 2 therefore approximately represents the inverse of the output resistance, R_{DS}, as a function of gate and drain voltages.

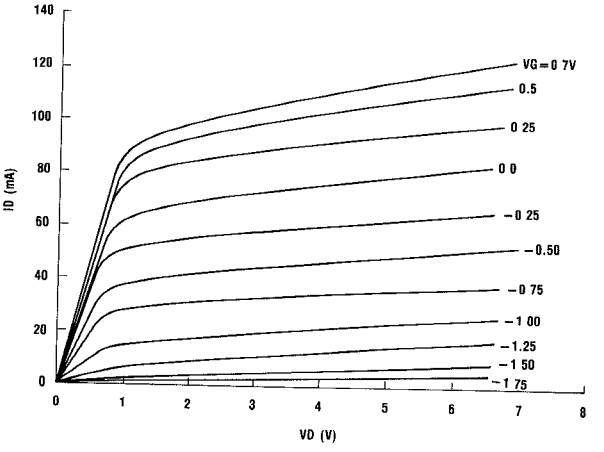

Figure 2. Drain current characteristic curves for 300 µm GaAs FET.

Previously, the nonlinear drain current source has been characterized by measuring the DC current that flowed into the drain of the FET as function of the known static gate and drain voltages. It has been shown, though, that the output resistance of a GaAs FET is a strong function of the frequency at which it is measured (2). In this reference, Camacho-Penalosa and Aitchison suggest that this is due to charge trapping effects at the epilayer-substrate interface. R_{DS} is seen to decrease with increasing frequency up to 100 KHz, after which it changes very little. The R_{DS} value measured at 1 MHz is

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typically 10 to 50 percent of the value at 10 Hz, depending upon the specific FET bias conditions. A plot of R_{DS} as a function of frequency for a 300 μm GaAs FET appears in Figure 3. The result of using incorrectly evaluated R_{DS} upon nonlinear model gain predictions is a consistent overestimation of small signal gain, compressed power output and harmonic content.

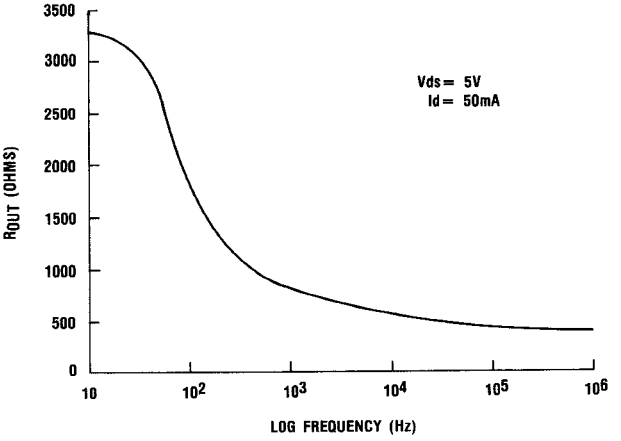

Figure 3. Output resistance of 300 μm GaAs FET as a function of frequency.

MEASUREMENT TECHNIQUE

In order to more accurately represent R_{DS} of an operating microwave FET, a technique of measuring the I_D nonlinear current source at 1 MHz has been developed. The test set, depicted in Figure 4, applies large signal half-sine waves to both the gate and drain of the transistor under test, while continuously monitoring the drain current. In this way, a path is taken through the FET operating curves similar to the path of Figure 5. The exact shape of the path depends on the relative phase of the drain voltage pulse with respect to the gate voltage pulse, with drain voltage lagging gate voltage shown in Figure 5. By varying this relative phase, the entire FET operating region may be mapped, as in Figure 6.

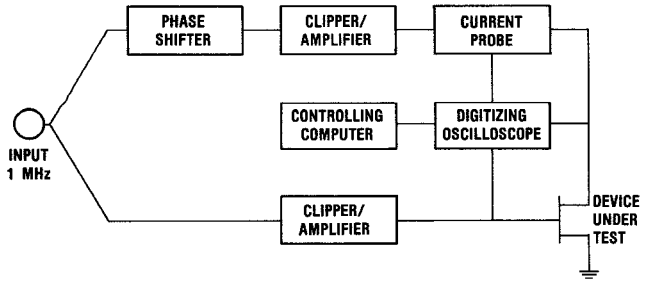

Figure 4. 1 MHz FET measurement test set.

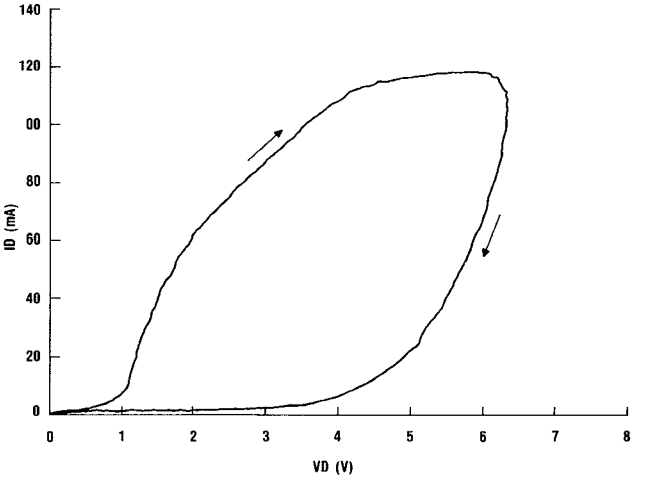

Figure 5. Typical path traversing operating region. This path shows drain voltage lagging gate voltage.

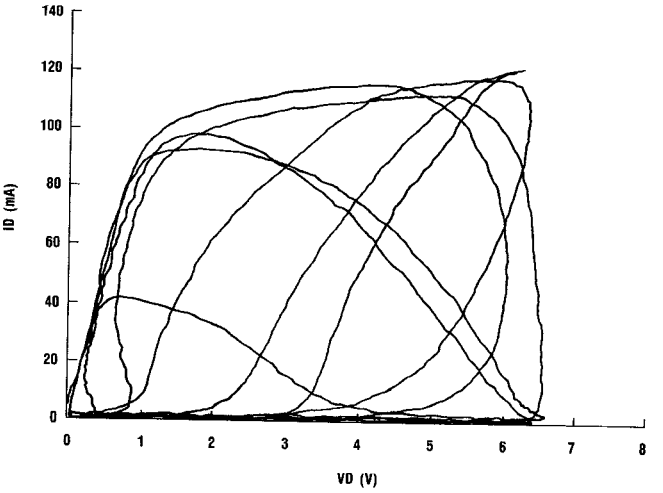

Figure 6. Entire mapping of FET operating region (7 curves).

At any one setting of relative phase, the gate and drain voltage and the corresponding drain current waveforms are displayed on a digitizing oscilloscope. The waveforms are then digitized and transferred to a local controlling computer. After the entire operating region has been mapped, involving about ten discrete settings of the drain voltage phase shifter, computer algorithms reduce the digitized data to FET characteristic drain current curves in the familiar form. Also produced is an I_D data table suitable for immediate use in the nonlinear modeling programs.

RESULTS

Results show that the error in gain and harmonic content calculations commonly encountered using I_D data derived from DC measurements has been greatly reduced. One

other advantage of the new technique is that it is fully automated, minimizing the time and effort involved in measuring devices.

Three circuits have been analyzed using data obtained by new technique. The first is a 300 μm GaAs FET measured in a 50-ohm system. Figure 7 is a plot of output power at the fundamental frequency and the first three harmonics vs. the input power at 4 GHz. Predicted fundamental power is within 1.0 dB of the measured value for input powers ranging from -20 dBm to +20 dBm, very accurately estimating linear and compressed gain as well as saturated power output. Harmonic power predictions are also very encouraging, showing correct trends, and being within 4 dB of measured values for all harmonics at power levels where they are significant. Figure 8 is an expanded plot of the same data presented in Figure 7 together with an additional calculation of harmonic power levels using a pulsed DC current measurement technique. As can be seen, the new measurement technique offers more accurate prediction of powers (about 1.5 dB improvement in fundamental power).

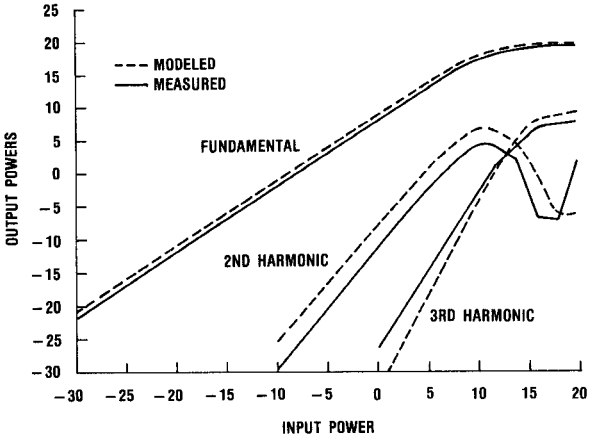

Figure 7. Output harmonic content for 300 μm GaAs FET in 50 ohm system, modeled and measured.

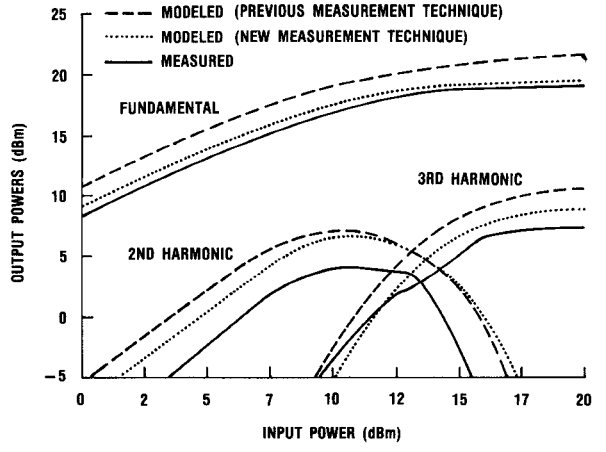

Figure 8. Comparison of modeled (new measurement technique versus previous measurement technique) and measured of output harmonic content for 300 μm GaAs FET in 50 ohm system.

The second circuit analyzed was a two-stage broadband monolithic power amplifier. The amplifier consists of two FETs of gate widths 900 and 1200 μm respectively, and input, output and interstage matching networks. Nonlinear current data was obtained for both FETs, and all matching networks were reduced to equivalent Z-parameter matrices. Using a version of the nonlinear circuit analysis program designed to iterate between the two stages, the entire circuit was simultaneously solved. As seen in Figure 9, both linear gain and saturated power output calculations agree with measured data with less that 1.0 dB error. Also, the amplifier 1 dB compression point is predicted to within 0.5 dB.

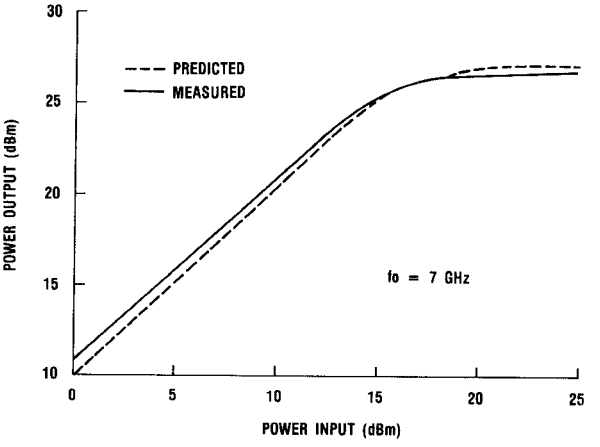

Figure 9. Comparison of predicted and measured output power of two-stage MMIC power amplifier.

Finally, an elemental mixer consisting of a 300 μm gate width FET connected to 50-ohm transmission lines on all ports was tested and analyzed. A 7 GHz RF signal was applied to the gate, a 6 GHz LO signal at 10 dBm was injected into the source, and the resulting 1 GHz IF signal was extracted from the drain. For this analysis, some modification of the nonlinear FET analysis program was necessary to include a third matching network at the source of the FET.

Power levels of the LO, RF, and IF frequencies appearing at the drain (output) of the device are seen in Figure 10, plotted as functions of the input RF power level. For the two leakage terms, predicted and measured values agree very well. Even for power levels well into mixer compression, less than 1 dB error is observed. Conversion loss predictions show a 4.5 dB worst case error, and are seen to very accurately represent measured small-signal conversion loss, a parameter which is impossible to predict with linear microwave CAD programs.

CONCLUSION

In conclusion, a method of accurately characterizing GaAs FET nonlinearities at RF frequencies has been developed and tested. Results show that the power output, compression

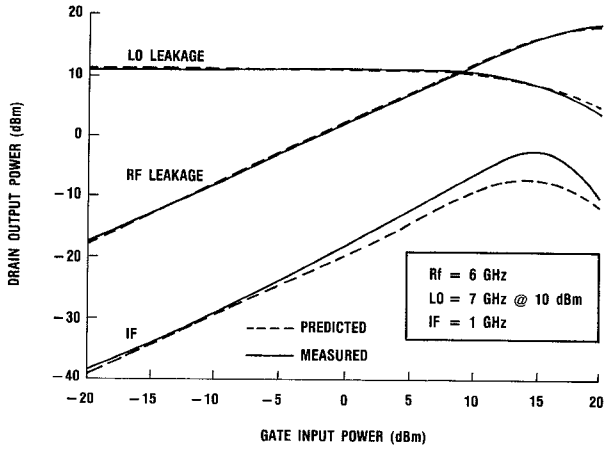

Figure 10. Measured and predicted performance of 300 μm FET mixer in 50 Ω system.

point, and harmonic content predictions of FET circuits are enhanced by the use of this measurement technique.

REFERENCES

(1) D. L. Peterson, A. M. Pavio and B. Kim, "A GaAs FET Model for Large-Signal Applications," IEEE Trans. on MTT, March 1984, pp. 276-281.

(2) C. Camacho-Penalosa and C. S. Aitchison, "Modelling Frequency Dependence of Output Impedance of a Microwave MESFET at Low Frequencies," Electronics Letters, Vol. 21, No 12, June 1985, pp. 528-529.